SURFACE INSULATION RESISTANCE TESTING OF SOLDERING PASTES AND FLUXES

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ABSTRACT
The broadening use of Surface Insulation Resistance (SIR) testing has brought about a need for a better understanding of the principles of SIR, a knowledge of proper techniques in testing, as well as an understanding of the common specifications governing this test. There are three basic reasons that SIR testing is run – to classify or qualify a product, to evaluate or control a process, or to compare materials or processes. The desired outcome in performing SIR testing is to determine if materials left following printed circuit board manufacture and assembly are likely to produce unacceptable current leakage levels or metal migration between conductors. SIR testing is a skill as much it is a science; proper sample preparation is key in producing an end product for test that simulates the manufacturing process. For the soldering paste or flux manufacturer, experimentation is often required to determine optimum process conditions for the material under test. Years of ongoing experimentation have led this laboratory to the development of a list of "helpful hints" not addressed in any of the test methods or specifications that may be applied to the testing of many types of materials. This article focuses solely on soldering fluxes and pastes and the methods used to evaluate them.

Key words: Surface Insulation Resistance, SIR, soldering paste, soldering flux,

INTRODUCTION
Imagine for a moment that it is 1962. You are an eighteen-year-old boy in the middle of a far off jungle in a war that you do not understand. There are explosions all around you and you are surrounded by a hostile enemy. You are knee-deep in water and mud, the humidity is overwhelming and the temperature strains your lungs. Your fear is only surpassed by your need to communicate with the helicopter assigned to extract your unit. Welcome to the infancy of Moisture and Insulation Resistance.

In the late 1950s and early 1960s, the United States Department of Defense (DOD) (specifically Ft. Meade) was charged with the task of developing specifications that would guarantee the effectiveness of field equipment employing the use of electronics and, specifically, printed circuit boards. Working in conjunction with the National Bureau of Standards and large companies like Honeywell, IBM and Boeing, the DOD presented the Tri-Services with several documents. Each of these documents was geared specifically to high-reliability electronic hardware, including: Naval Electronic Communications, Electronic Ground Equipment, and Electronic Airborne, to name a few.[1]

Within these documents rested various test and property requirements deemed as critical to the successful operation of the field hardware. Properties such as Thermal Stress, Thermal Shock, Vibration and Fungus Resistance were at the top of the list of "mission critical" parameters. At the time, however and given the environment of the present conflict, none were considered more critical than Moisture and Insulation Resistance.

In the thirty years since the war in Vietnam, it is hard to imagine there could be a more critical need than protecting the lives of servicemen. However, today's high-speed, densely populated electronic hardware configurations demand more complex testing than their first generation cousins. In the case of Moisture and Insulation Resistance testing, "simply" measuring electronic capabilities at various intervals during the test is no longer sufficient. Designers and manufacturers must guarantee their product throughout the entire environmental exposure (in the field and in the test protocol). It is this requirement that has driven the need for ongoing monitoring of product during environmental exposure and the sophisticated, yet limited, test methods which support it.

Surface Insulation Resistance (SIR) tests were first performed on printed circuit board (PCB) base materials. As the PCB industry's designs and materials became more complex, SIR testing became a part of material and process qualifications.[2] For those who are new to the field of electronics, the question is often asked:

WHY SHOULD I PERFORM SIR TESTING?
SIR testing is performed to determine whether the materials used in an assembly are likely to produce unacceptable current leakage levels, or shorts due to metal migration between conductors. This metal migration is best described as a reverse plating of the copper or tin-lead conductors in the presence of ions, water, and an electrical potential.[3]

What does this mean in terms of the final product? Metal migration between isolated conductors on a completed assembly may produce electrical shorts. In simple terms, shorts occur when the space between the conductors is bridged by dendrites formed by re-deposited metal ions (photo 1). This occurrence spells FAILURE.

SIR testing is performed on a variety of circuit board materials. Although the detailed information contained in this article pertains to soldering fluxes and pastes, many of the helpful hints apply to other products as well. SIR testing is most often performed for one of the following three reasons:

1. As part of a qualification or classification of a product
2. To evaluate or control a process
3. To compare materials or processes.

First, when marketing products to everyone from bare board fabricators to PCB assemblers to original equipment manufacturers (OEM's), evidence is often required that the product in question (e.g. laminate, solder mask, conformal coating, solder paste or flux, etc.) meets typical industry standards or customer generated specifications. Common specifications used to test soldering pastes and fluxes include IPC, Bellcore (Telcordia), and Japanese Industrial Standards (JIS). The ANSI/J-STD-004 document *classifies* fluxes or the flux component of soldering paste, cored wire, and preforms. The flux is characterized as RO (rosin), RE (resin), OR (organic) or IN (inorganic). The flux activity level is specified as L0, L1 (low), M0, M1 (medium), H0 or H1 (high). Various test methods, including SIR, are used to determine the activity level of the material under test. Other specifications, Bellcore and JIS for example, have *pass/fail* criteria for the soldering paste or flux. These criteria must be met before the manufacturer can add this specification to the list that his product meets. It is important for manufactures to meet as many industry and consumer standards as possible to increase the marketability of their product.

Whether or not a flux or paste meets the requirements of a specific industry standard is one of the first criteria a potential buyer uses in selecting this new product. If the new flux/paste does not meet the standard, it is often first to be eliminated from consideration. This means lost business to the flux or paste manufacturer.

The second reason SIR testing may be performed is to evaluate or control a process. During process development, extensive testing may be performed at various process stages, including inner signal layers of multilayer boards, bare printed wiring boards (PWBs), PWBs after hot air solder leveling (HASL) or other surface finish, and assembled PWBs after solder paste and reflow, wave solder, and cleaning. Results from well-documented process development testing can later be used as a baseline for periodic process control testing. These baseline results can also be extremely useful during failure analyses if problems are experienced during assembly production or use.

The third reason SIR testing is performed is to compare materials or processes. Often, manufacturers want to change one or more materials in their current board manufacturing process to decrease costs or to eliminate process steps (e.g. clean to no-clean). They need to assess the impact of this change on current leakage and reliability. This may be accomplished via indirect or direct comparison of the old and new materials or processes.

An indirect comparison may be made by using standard test vehicles and test methods to enable valid comparisons of results from tests conducted at different times or locations. This is especially useful if one product within the manufacturing process is being considered for replacement. For instance, product X is being considered over product Y because it is less expensive, but Bellcore standards must be met. Direct and indirect comparisons of products allow the evaluator to make the best decision in his manufacturing process.

A direct comparison may be made by testing various materials or processes *simultaneously*. When a direct comparison is performed, industry test methods may be modified to better suit the manufacturer's needs. A list of typical modifications is included below. The tester must understand that because the test method is being modified, the pass/ fail criteria, such as minimum SIR value, may no longer apply. Evaluation consists of comparing the results for test samples representing the old and new processes.

TYPICAL METHOD MODIFICATIONS:

1. Variations to test vehicle
   a. Finer conductor widths and spaces
   b. Alternate *comb* patterns (typical comb pattern – photo 2)
   c. Addition of components
   d. Alternate base material or surface finish
   e. Use of production board
2. Process steps performed exactly as manufacturer intends (E.g. application of flux, preheat)
3. Non-standard temperature and/or humidity
4. More than one temperature and humidity within one test profile
5. Longer or shorter test duration
6. More frequent to continuous monitoring of SIR

Those companies on the forefront of product evaluation take SIR testing a step beyond the routine. With the printed circuit board industry moving to a fine-pitched product with micro-ball grid arrays (BGAs), there is a need to evaluate the potential problems associated with this move. The potential for shorts increases with the finer spaced, no-clean processes being used under micro-components. Those companies in need of the most reliable PCB possible want to evaluate what effect these board changes will have on long term performance. PCBs that are used in medical products or avionics for example often put people's lives at risk in the event of even an intermittent failure.

Because an intermittent failure may cause disastrous outcomes, companies want to evaluate the exact steps they use in their processes via an accelerated reliability test. Manufacturers may choose to evaluate their process using

an SIR test with a ramping of temperature and humidity because they want to simulate the exposure of their product in the field. PCBs are used in products that are exposed to environments that range from cold and dry to hot and moist, often vacillating between the two. Other manufacturers may want to move towards continuous monitoring because they understand that dendrites can form and disappear in the space of 20 minutes. As we now know, even an intermittent short could cause a plane to crash or a heart/lung machine to stop.

Leading companies that are not satisfied with typical industry standards, understand the potential for disaster and are working to improve test methods and specifications to avoid these problems in the future.

THE NEXT QUESTION: WHAT TYPE OF TEST SHOULD I RUN?

There are several industry standards that include methods for Surface Insulation Resistance testing. Knowing where and how your solder paste or flux will ultimately be used will aid in choosing the proper specification for testing. A summary of some frequently used and widely accepted test methods is included at the end of this article.

What test conditions will best assess the performance of my flux or paste? Test conditions range from worst-case actual use conditions to determine leakage current levels (e.g., 35°C/85%RH, no bias), to more severe conditions that accelerate reactions and encourage metal migration (e.g., 65°C/85%RH or 85°C/85%RH with bias). Tests at increased temperatures can give an indication of the long-term performance of the material or process, but temperatures that are too high can change the nature of and behavior of the tested materials.

More customers are demanding SIR tests which subject the samples to a variety of sequential conditions. However, this type of testing requires some know-how. Care must be taken when altering temperature/humidity conditions in order to prevent moisture condensation on the test patterns. Temperature must be increased before humidity and humidity decreased before temperature. If an electrical bias is applied to the test patterns while chamber conditions are changed, the chamber must be ramped slowly. Metal migration (formation of dendrites) occurs very rapidly under bias if moisture condenses on the test or control patterns.

HOW CAN I ENSURE VALID SIR RESULTS?

Below are some helpful hints (issues to consider) in board preparation. The "best methodology" will vary from material type to material type.

- Test boards should be visually examined prior to use. Care should be taken to confirm that proper widths and spaces were maintained during manufacturing. Boards should be rejected if they have any type of stains or debris on the surface.

- Use a high-quality substrate for the test boards to obtain the best results possible. Bare board controls from the same lot of test boards should always be run with an SIR test. These controls, thoroughly cleaned, monitor laminate quality as well as chamber conditions.

- Do not assume that boards are clean following manufacture. If a material is to be tested, you must start with pre-cleaned test boards; otherwise, you are testing the board vendor's process. If no pre-cleaning procedure is included in the specification to be used, follow the pre-cleaning procedure in IPC-TM-650, method 2.6.3.3[4] or IPC-9201[6]. Do not substitute tap water for deionized water during cleaning or rinsing. After the boards have been thoroughly dried, take initial IR readings to verify the cleaning procedure and board quality.

- If boards are to be stored after cleaning, place them in a clean desiccator. Special bags that are contaminant-free, work well for clean board storage and shipment. Other types of bags may contain slip agents or other substances that can end up on the board surface.

- <u>Every</u> SIR test should include controls to enable comparison of results for tested materials or processes with results for clean, bare substrates. If a process is being tested, "as-received" boards from the vendor (representing the starting point for the process) should also be included in the test.

- Pastes and fluxes vary in performance; therefore, extra time, sample, and cleaned test boards should be set aside for experimentation. When possible, have a conversation with the manufacturer to help determine how the material behaves (i.e., what preheat times and temperatures work best, how viscous is the material, what is the best way to clean the material if it is to be cleaned?).

Liquid Fluxes:

- The preheat temperature and duration prior to soldering can be critical to prevent bridging and webbing. Current industry standards do not address preheating at all.
- Soldering boards by "floating" them on a solder pot produces good test specimens with the proper technique. Practice and frequent dross removal are key. Preparing bare copper samples on a wave solder machine can be just as challenging as using a solder pot, and does not guarantee the absence of solder webbing or bridges.

Flux Pastes (Solid Flux):

- If the flux paste will not readily dissolve in isopropanol or the manufacturer recommended

solvent(s), it can usually be stenciled onto the comb patterns. Use a low-heat hot plate as your work surface to keep the paste soft enough to stencil.

Flux-Cored Solder Wire:

- The key to applying solder wire to a comb pattern is a clean, appropriately sized soldering iron tip and a steady hand. An experienced solderer is your best bet.

Pastes:

- Many new pastes on the market appear to require a thinner stencil to eliminate solder bridging and bulging (photo 3); yet typical industry standards (IPC[5] and Bellcore[7]) specify use of a 0.008" (0.2 mm) stencil. Sometimes the only way to produce good test boards using the thicker stencil is to modify your squeegee technique to achieve a thinner application of paste onto the comb patterns. Solder bridges must be eliminated, and bulges, though not a guarantee of low SIR readings, have been observed to intensify reactions in the flux residues.

Miscellaneous Concerns:

- The post-solder cleaning procedures listed in current test methods are not sufficient for some fluxes. You may wish to modify the test method, and document the actual cleaning procedure in the final report.
- Based on experience, small solder balls (photo 4) do not usually yield decreased IR results. However, solder webbing definitely causes low IR readings.

WHAT DOES IT MEAN?

The industry standards summarized at the end of this article include required minimum or average insulation resistance values under test conditions. In addition, the standards require a visual examination of the test boards after they are removed from the test chamber. This visual examination is as important as the resistance readings, but may be de-emphasized because it is tedious and time-consuming. The visual exam is critical for several reasons:

1. Dendrites can bridge the gap between conductors and be destroyed by the resulting high current flow during the relatively long intervals between test measurements. The resistance measurements may not reflect the temporary existence of the dendrite(s), but the post-test visual examination should produce evidence of the short in the form of carbonized debris that bridges between conductors.[8]

2. Isolated low readings may be the result of an anomaly not associated with the materials or process being tested. Examples of such anomalies are damage to the substrate, fibers, particles, or other isolated foreign contamination. Most standards allow a certain number of the test points to be omitted due to visible reasons of this nature.

The visual exam can reveal evidence of interactions of residues with metallization or other board materials. Reaction products that do not degrade the SIR below acceptable limits during the course of testing may still be unacceptable to the customer. Be sure that all visible anomalies and changes are reported, even if they do not constitute a failure, as defined by the test specification. Be aware that standards are not in agreement and frequently are not clear in their definitions of unacceptable visible anomalies. Insist that photographs of anomalies be included in the final test report.

If the material or process sample boards fail to meet minimum SIR requirements, check the control board readings. If the clean bare board controls also fail, inadequate chamber control, instrument malfunction, or chamber contamination should be suspected and the test should be repeated. If the "as-received" boards fail, the vendor's cleaning and handling processes should be questioned. The quality of the substrate can also affect test results.

In summary, judicious investment of time and money in Surface Insulation Resistance testing, using proper techniques to yield valid results, may stimulate business interest, lessen the chance of field failures, and promote more efficient production of printed circuit boards or assemblies.

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[Note: Bracketed entries in the following tables are not required by the specification, but have been used successfully or are recommended by the authors.]

Summary of SIR Specification Requirements	
Bellcore GR-78-CORE, Issue 1[9] **Flux, Solder Paste** (Section 13.1) **SIR** Test Pattern = Bellcore Figure 14-1 - 50 mil (1.3 mm) space or IPC-B-25 B or E - 12.5 mil (0.3 mm) space or [IPC-B-25A D - 12.5 mil (0.3 mm) space] or Other with squares count > 110 (must calculate requirement)	
Number of patterns:	
Liquid Flux, CLEAN = 9 [+3]	[3 control bare] 3 pattern up solder pot uncleaned 3 pattern down wave or fountain uncleaned 3 pattern down wave or fountain cleaned
Liquid Flux, NO CLEAN = 6 [+3]	[3 control bare] 3 pattern up solder pot uncleaned 3 pattern down wave or fountain uncleaned
Solder Paste, CLEAN = 6 [+3]	[3 control bare] 3 stenciled and oven reflowed cleaned 3 stenciled and oven reflowed uncleaned
Solder Paste, NO CLEAN = 3 [+3]	[3 control bare] 3 stenciled and oven reflowed uncleaned
Cored Wire, CLEAN = 6 [+3]	[3 control bare] 3 hand soldered cleaned 3 hand soldered uncleaned
Cored Wire, NO CLEAN = 3 [+3]	[3 control bare] 3 hand soldered uncleaned
Heat profile:	
Solder pot, wave, or fountain =	260±6°C
Oven reflow =	Customer profile or [3 minutes in 165°C passive air oven followed by 60 seconds in 250°C forced air oven]
Solder Leads With:	R or RMA flux cored solder wire, uncleaned; shield patterns
Test Conditions =	35±2°C, 85% minimum RH
Take Resistance Measurements at:	[Initial] 24 hours 96 hours
Current Limiting Resistors =	[1MΩ]
Measurement Voltage =	+100 VDC for 1 minute
Bias Voltage =	-50 VDC applied at 24 hours and maintained until 96 hours
Requirement =	Geometric Mean (logarithmic form) of test measurements of each sample group at 24 hours and 96 hours must be: $\geq 1 \times 10^{11}$ Ω (50 mil space, 110 squares, Figure 14-1) or $\geq 2 \times 10^{10}$ Ω (12.5 mil space, 528 squares, IPC-B-25 B or E) or $\geq 2 \times 10^{10}$ Ω (12.5 mil space, 528 squares, IPC-B-25A D) or $\geq 1 \times 10^{10}$ Ω (20 mil space, IPC-B-24 pattern, 1040 squares)

"Assignable cause" low resistances can be omitted provided 10 (of original 12) test points are included in the average.
No discoloration (green, blue-green, blue, or blue-black) of the conductors.

IPC-TM-650, 2.6.3.3 A and ANSI J-STD-004 (1995)[10] **Flux, Solder Paste** **SIR**	
Test Pattern =	IPC-B-24 - 20 mil (0.5 mm) space, 4 per board
No. boards:	
Liquid Flux, CLEAN = 3 + 2	2 control bare 3 pattern down solder pot or wave cleaned
Liquid Flux, NO CLEAN = 6 + 2	2 control bare 3 pattern up solder pot uncleaned 3 pattern down solder pot or wave uncleaned
Solid Flux, CLEAN = 3 + 2	Dilute to 35% by weight solution in appropriate solvent; test as Liquid Flux, CLEAN.
Solid Flux, NO CLEAN = 6 + 2	Dilute to 35% by weight solution in appropriate solvent; test as Liquid Flux, NO CLEAN.
Solder Paste, CLEAN = 3 + 2	2 control bare 3 stenciled and oven reflowed cleaned
Solder Paste, NO CLEAN = 3 + 2	2 control bare 3 stenciled and oven reflowed uncleaned
Cored Wire, CLEAN = 3 + 2	Extract per ANSI J-STD-004, paragraph 4.7.6.1 and dilute to 10% by weight solution; test as Liquid Flux, CLEAN.
Cored Wire, NO CLEAN = 6 + 2	Extract per ANSI J-STD-004, paragraph 4.7.6.1 and dilute to 5% by weight solution; test as Liquid Flux, NO CLEAN.
Heat profile:	
Solder pot =	245 - 260°C for 4 ± 1 seconds
Solder wave =	245 - 260°C for 3 ± 1 seconds
Oven reflow =	Customer profile or [3 minutes in 165°C passive air oven followed by 60 seconds in 250°C forced air oven]
Solder Leads With:	R flux and solid solder wire, uncleaned; shield patterns
Test Conditions =	85±2°C, 20% RH for 3 hours Ramp to 85±2% RH over 15 minutes minimum Stabilize 1 hour minimum before bias
Take Resistance Measurements at:	[Initial] 24 hours 96 hours 168 hours
Current Limiting Resistors =	[1 MΩ]
Measurement Voltage =	+100 VDC for 1 minute
Bias Voltage =	-45 to -50VDC applied at 4.5 hours and maintained until 168 hours (except during readings)
Requirement =	Control board readings at 96 and 168 hours must be ≥ 1 x 10^{09} Ω.

Per ANSI J-STD-004, resistance readings at 96 and 168 hours must be ≥ 1 x 10^{08} Ω.

“Assignable cause” low resistances can be omitted (up to 2 readings for a given condition).

No dendrites that reduce conductor spacing by 25% or more, at 10X to 30X with backlighting. Report corrosion and dendritic growth.

JIS Z 3284[12], Annex 3 Solder Paste Electric Insulation Resistance Test		
Test Pattern =	Type 2 (0.318 mm width, 0.318 mm space, 15.75 mm overlap) copper comb patterns on GE-4 substrate with initial readings of $\geq 1 \times 10^{13}\Omega$	
No. boards:	[1 control] Three 5-point test patterns	
Heat profile:	Heat in oven at 150°C for 2 minutes then reflow for 30 seconds on hot plate at 260°C. Clean if needed per Annex 13.	
Solder Leads With:	Not Specified	
Test Conditions =		
A	40±2°C and 90-95%RH for 168hours	
B	85±2°C and 85-90%RH for 168 hours	
Take Resistance Measurements at:	Initial, 24, 96 and 168 hours	
Current Limiting Resistors =	None required	
Measurement Voltage =	100 VDC for 1 minute	
Bias Voltage =	None	
Requirement = (Geometric Mean)	Condition A	Condition B
Low Activity	$\geq 1 \times 10^{11}\Omega$	$\geq 5 \times 10^{8}\Omega$
Medium Activity	$\geq 1 \times 10^{11}\Omega$	$\geq 1 \times 10^{8}\Omega$
High Activity	$\geq 1 \times 10^{11}\Omega$	$\geq 1 \times 10^{8}\Omega$

Low IR measurements due to abnormalities such as water drops or lint shall be deleted. Temporarily decreased IR readings at 24 or 96 hours shall also be deleted.

Other common specifications for the testing of soldering pastes or fluxes include DIN-32513, ISO 12224-1, and JIS Z 3197.

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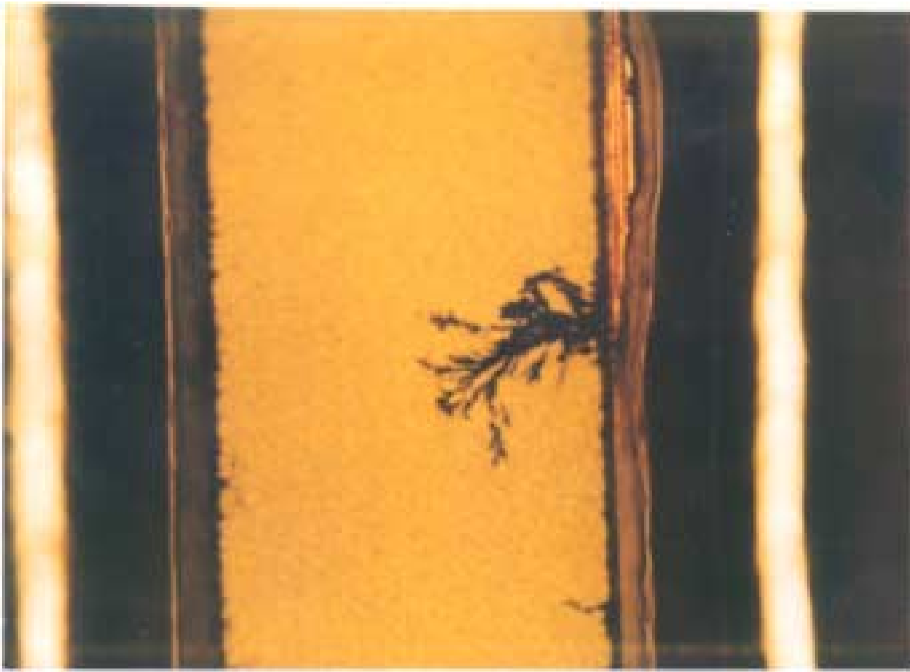

Photo 1: Example of a dendrite (100x)

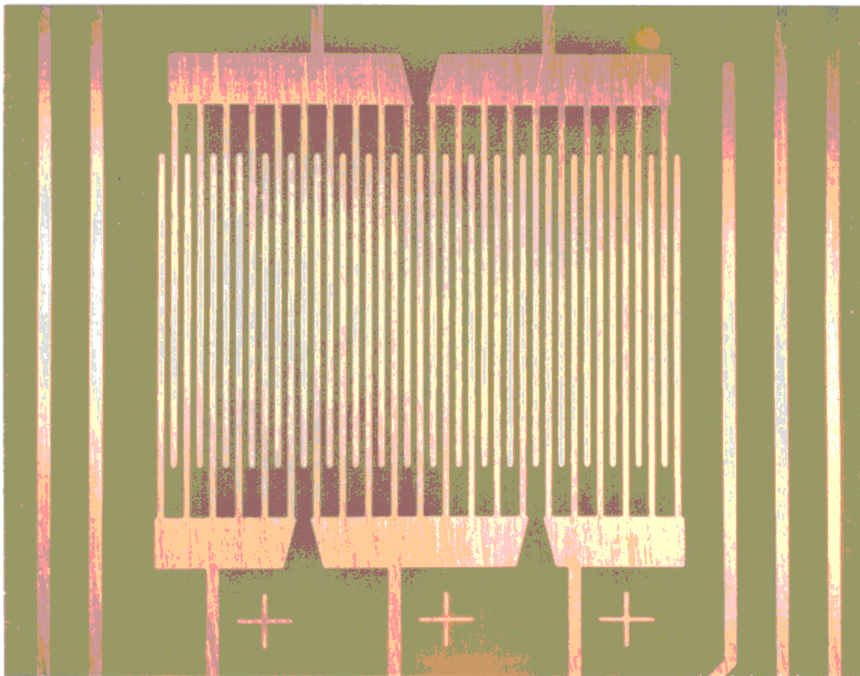

Photo 2: Example of a typical test pattern, IPC-B-25A, D-comb (≈2.5x)

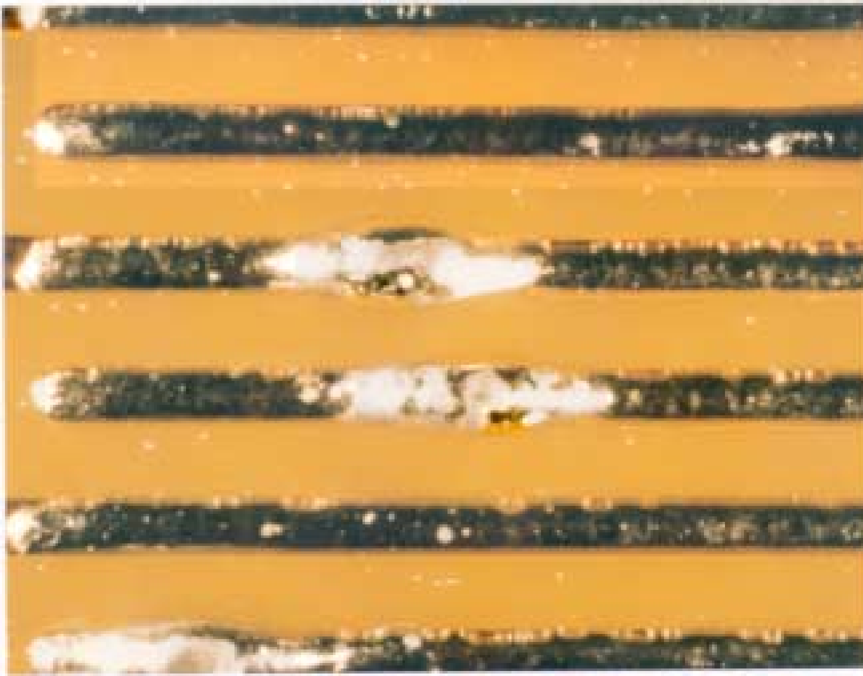

Photo 3: Example of solder bulges (≈20x)

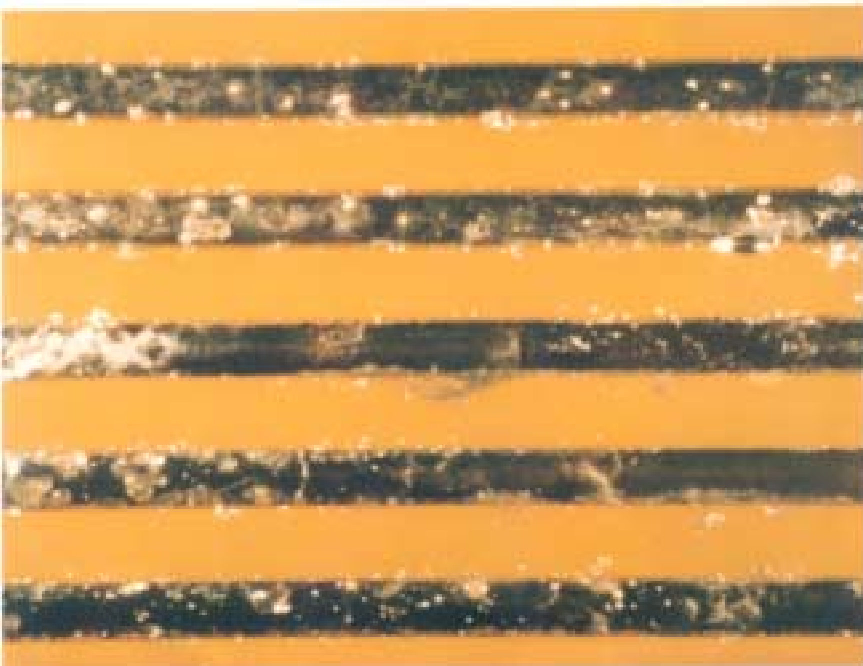

Photo 4: Example of solder balls, solder debris present between traces (≈20x)